Amendments to Specification

Please replace paragraph 0029 with the following paragraph:

If it is assumed that the DDS operation clock frequency is 196.608 MHz, the output frequency is 58.9824 MHz and the number N of input bits of phase accumulator 102 is 48, then it becomes ~~59.9824~~ 58.9824 MHz=FTW*196.608 MHz/2^{48} when applying the above equation (1). Therefore, the FTW is (58.9824 MHz*2^{48})/196.608 MHz. By equation (2), the FTW becomes 4CCCCCCCCCCD in hexadecimal, or 010011001100110011001100110011001100110011001101 in binary.